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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael Goessel et al.

APS Rec'd PCT/PTO 17 FEB 2006

Serial No.: Unknown
(Priority Application No. DE 103 38 922.9)
(International Application No. PCT/DE2004/001799)

Filed: Herewith
(Priority Date August 20, 2003)
(International Filing Date August 11, 2004)

Docket No.: I431.151.101/FIN 504 PCT

Title: ELECTRICAL DIAGNOSTIC CIRCUIT AND METHOD FOR THE
TESTING AND/OR THE DIAGNOSTIC ANALYSIS OF AN
INTEGRATED CIRCUIT

INFORMATION DISCLOSURE STATEMENT

Mail Stop PCT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, it is respectfully requested that this Information Disclosure Statement be entered and the documents listed on attached form 1449 be considered by the Examiner and made of record. Any required copies of patents, publications or other documents are enclosed for the Examiner's review. Pursuant to the provisions of M.P.E.P. 609, Applicants further request a copy of the 1449 form, marked as being considered and initialed by the Examiner, be returned with the next Official Communication.

Since this Information Disclosure Statement is being submitted within three months of filing national application; or date of entry of national application; or before the mailing date of the first Office Action on the merits, a fee has not been enclosed. However, if such fee is required, the Patent Office is hereby authorized to charge Deposit Account No. 500471 for fees as set forth under 37 C.F.R. 1.17(p).

Information Disclosure Statement

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Applicants respectfully request consideration of these references during prosecution of the above-identified matter. The Examiner is invited to contact the Applicants' representative at the below-listed telephone number if there are any questions regarding this Communication or the tendered references.

Respectfully submitted,

Michael Goessel et al.,

By their attorneys,

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Dated: February 17, 2006
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CERTIFICATE UNDER 37 C.F.R. 1.10:

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Date of Deposit: February 17, 2006

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By Vanessa Carels
Name: Vanessa Carels

IAP5 Rec'd PCT/PTO 17 FEB 2006

FORM PTO-1449	Docket No.: I431.151.101/FIN 504 PCT		Serial No.: Unknown Priority Appln. No. DE 103 38 922.9 Int'l Appl. No. PCT/DE2004/001799
	10/568842		
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Applicant: Michael Goessel et al.		
	Filing Date: Herewith Priority Date 20 August 2003 Int'l Filing Date 11 August 2004	Group Art: Unknown	

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

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	✓	P.H. Bardell, W.H. Mc Anney und J. Savir, "Built-In Test for VLSI: Pseudorandom Techniques", New York, 1987, pgs. 285-287.
	✓	M. Abromovici, M.A. Breuer, A.D. Friedman; "Digital Systems Testing and Testable Design", Computer Science Press, pgs. 365-382.
	✓	L. Voelkel, J. Pliquet; "Theore-tische Grundlagen und Probleme - Ausblick und Anwendungen"; Akade-mie-Verlag Berlin 1988 Standard Literature.
	✓	Shu Lin, D.J. Costello; "Error Control Coding, Fundamentals and Applications", New Jersey 07632 pgs. 79-85.
	✓	Gerner, M. Muller, B.: Sandweg, G.: "Selbsttest digitaler Schaltungen. Munchen (u.a.): Oldenbourg, 1990, p. 100-117, 140-151.
	✓	Internet Page http://www.adobe.com/products/acrobat/readste2.html of December 17, 2001 (reconstructed by http://www.archive.org)

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.